REMARKS

The claim amendments made in this Preliminary Amendment address each of the rejections made in the parent case (U.S. Patent Appl. No. 10/167,754). By addressing the rejections via this Preliminary Amendment, each of the claims of the present application are in condition for final allowance.

Regarding the claims of the parent application, the Examiner noted a "missing interconnection" on the source or drain side of the write device. Specifically, the Examiner noted that the phrase "another of the data line" should be amended to "another the data line." It is submitted that Applicant's language was both more grammatical correct, and, in fact, the proper way to claim the proposed interconnection.

However, in an effort to forward prosecution of the claimed invention, Applicant has chosen to include with the reference to the second of the plurality of data lines the recitation of "a second one of said data lines" in the claims of the present application. This recitation is believed to address the Examiner's concerns, whereby the claims in this application are in condition for final allowance.

Prior Art Issues

In the parent application, the Examiner rejected the claims under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,803,664 to Itoh ("Itoh") by itself or in view of U.S. Patent No. 5,492,851 to Ryou ("Ryou") or U.S. Patent No. 5,977,591 to Fratin ("Fratin"). Each of these "obviousness" rejections is overcome by the claims presented herewith.

Specifically, the Examiner in the parent case held that Itoh discloses all of the claimed subject matter except for the SOI thickness and then asserted that TFT transistors are well known and the film channel (57) would be obvious to one of skill in the art. However, the phenomenon of a low leakage current associated with a channel thickness below 5nm in a TFT structure was not heretofore known, and Itoh would not lead one to this invention. In fact, no other known entity has produced and used a 5nm channel, as a TFT is normally fabricated by doping impurities in the source or drain region in a polysilicon film with the same film thickness along the source to drain. If this conventional method is conducted in a very thin polysilicon film (as in the present invention), it is difficult to make contact with the source or drain. The present invention provides for ready contact with a "thickly" fabricated source or drain region with only the channel region being thinly formed (e.g., below 5nm).

Each of the independent claims in this case includes a specific recitation of this distinguishing feature. As such, each of the claims herein distinguish over Itoh and are in condition for final allowance.

With respect to Fratin and Ryou, these references provide no additional teachings that, in combination with Itoh, render the present claims unpatentable. For example, the present invention as claimed includes two transistors in each memory cell (p-channel and n-channel) while Fratin uses a transistor including an n-type and p-type impurity into a single gate of a single transistor. Ryou utilizes a TFT as an upper level DRAM cell and a bulk silicon MOSFET as a lower DRAM cell, the upper cell formed on the lower cell with both cells performing the same function. The TFT on the upper cell has a large leakage current compared to the lower cell. The present invention, on the other hand, uses an extremely low leakage current thin film TFT for charge storage and a MOSFET as a read transistor, the two transistors performing different functions, as claimed.

Applicant hereby requests that the above Preliminary Amendment be entered and considered before taking up the present application for prosecution on the merits. In order to further prosecution of the present application, Applicant has addressed each of the issues raised by the Examiner in an Office Action filed in the parent case to put each of the claims

in the present case in condition for final allowance. Prompt notice to such effect is respectfully requested.

Respectfully submitted,

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